

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Wayne F. Ellis et al.

Serial No.: 10/707,797

Filed: January 13, 2004

Title: Integrated Redundancy Architecture And Method for Providing Redundancy Allocation
to an Embedded Memory System

Attorney Docket No.: BUR920030151US1
(02016-00170)

Group Art Unit: 2117

Confirmation No.: 1796

Examiner: Guerrier Merant

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

August 28, 2008

**RESPONSE TO FINAL OFFICE ACTION AND PRELIMINARY AMENDMENT FOR
FIRST REQUEST FOR CONTINUED EXAMINATION**

This is in response to the Office Action mailed from the United States Patent and
Trademark Office on May 28, 2008, with respect to the above-identified application.

A **Status of the Claims** starts on the following page 2.

Remarks concerning the Office Action start on the following page 7.